Joint Mapping of Mobility and Trap Density in Colloidal Quantum Dot Solids

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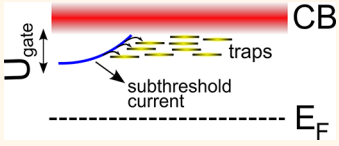
ABSTRACT Field-effect transistors have been widely used to study electronic transport and doping in colloidal quantum dot solids to great effect. However, the full power of these devices to elucidate the electronic structure of materials has yet to be harnessed. Here, we deploy nanodielectric field-effect transistors to map the energy landscape within the band gap of a colloidal quantum dot solid. We exploit the self-limiting nature of the potentiostatic anodization growth mode to produce the thinnest usable gate dielectric, subject to our voltage breakdown requirements defined by the Fermi sweep range of interest. Lead sulfide colloidal quantum dots are applied as the active region and are treated with varying solvents and ligands. In an analysis complementary to the mobility trends commonly extracted from field-effect transistor studies, we focus instead on the subthreshold regime and map out the density of trap states in these nanocrystal films. The findings point to the importance of comprehensively mapping the electronic band- and gap-structure within real quantum solids, and they suggest a new focus in investigating quantum dot solids with an aim toward improving optoelectronic device performance.



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Colloidal quantum dots (CQDs) combine processing from the solution phase with wide-ranging tunability of the band gap *via* the quantum size effect. These attractive qualities have led to intensive study of these materials in optoelectronic device applications ranging from light-emitting devices[1] to photodetectors[2,3] and photovoltaics.[4−8]

In parallel, much effort has been invested in elucidating the mechanisms of electronic transport in colloidal quantum dot solids and in using these insights to inspire new strategies to improve charge carrier mobility. Here, the rate of progress has been remarkable. Whereas reported mobilities did not reach above 10^{-3} cm^2 V^{-1} s^{-1} before 2005,[9] advances in the materials chemistry of quantum dot solids have led to field-effect transistor (FET) mobilities greater than 10 cm^2 V^{-1} s^{-1}.[10−12]

Paradoxically, breakthroughs in reported FET mobilities have yet to translate into the expected advances in optoelectronic device performance. While tighter packing, bifunctional ligand approaches, and closer inter-dot distances are considered key strategies to improve mobilities, trap states in colloidal quantum dot films continue to be a dominant mechanism in triggering nonradiative recombination and limiting device performance.[6]

We took the view that FET-based investigations could provide a more complete picture of the transport behavior of quantum dot films—a picture that went beyond mobility alone and provided crucial information about the shallow trap state regime. Specifically, in carefully architected FET devices, the subthreshold swing of the transfer characteristics contains key evidence of the density of trap states within the band gap. We therefore desired a method of probing the density of states in the energy region that lies between the equilibrium Fermi level and the majority band edge.

RESULTS AND DISCUSSION

FET studies of colloidal quantum dot solids have typically employed thick, low-permittivity dielectrics as the gate oxide (Figure 1a, bottom-right corner, SiO_2 case). In this case, a preponderance of the applied bias falls across the dielectric, and only a small—and imprecisely known—potential

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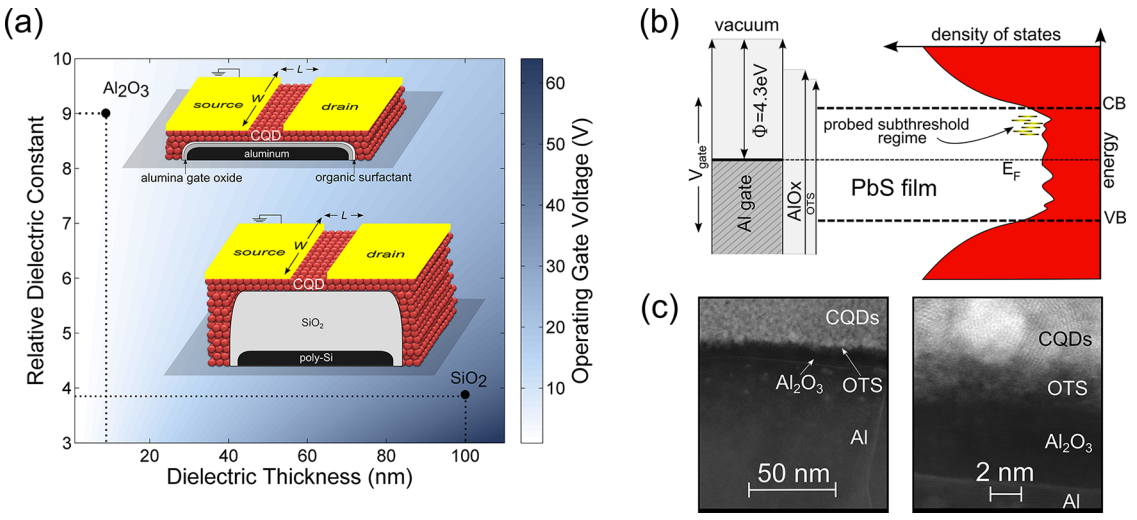

Figure 1. (a) Operating gate voltage (color scale) required to achieve one charge carrier per quantum dot (equivalent to a density of approximately 10^{13} cm^{-2}) for varying gate oxide dielectric constants and thicknesses. The thin (8 nm) electrochemically grown aluminum oxide (ε_r = 9) plus octadecyltrichlorosilane (OTS) capping monolayer (top inset) results in an order of magnitude lower gate voltage operation compared to typical 100 nm+ silicon dioxide (ε_r = 3.9) (bottom inset). (b) Band diagram showing a schematic density of states in the quantum dot film on the right. We sweep the gate voltage to probe the energy states above the Fermi level and below the conduction band onset of our n-type films. (c) Transmission electron microscope (TEM) cross section of our device shows an approximately 8 nm thick alumina gate dielectric capped with a 2−3 nm thick monolayer of OTS.

drop occurs within the quantum dot film under study. To illustrate, gate biases in the range of 50−100 V are required for significant modulation of source−drain conductance,[9,10] while the Fermi level inside the quantum dot film is moved only by a few hundred millielectronvolts when this wide gate bias swing is applied.

We therefore pursued instead an approach that would produce the minimum-needed gate dielectric thickness and would maximize its permittivity. Employing a thin, high dielectric constant gate insulator, we maximize the amount of bias that falls across the quantum dot film, all with the goal of ensuring a more direct mapping of applied V_g variation onto $e \cdot E_F$ movement (Figure 1b). Now, the preconductive subthreshold regime is on the order of a few hunded millielectronvolts—an upper bound for the actual Fermi energy of the quantum dot film. For exact gate voltage to vacuum potential correlations, techniques such as ultraviolet photoelectron spectroscopy (UPS) can be used in conjunction with the methods detailed in this article.[13]

We construct CQD field-effect transistor (FET) structures that rely on a double-layer gate dielectric made of 8 nm anodically grown alumina (Figure 1a, top-left corner, and Figure 1c, transmission electron microscope images) terminated using an aliphatic C_{18} passivation monolayer. This strategy, adapted from organic FETs, results in a dot−dielectric interface that is well-defined and trap-minimized such that residual energy states can be assigned as an upper limit to the traps in the quantum dot film.[14]

The nanodielectric approach minimizes the operating driving voltages, enabling comparison of the gate potential and Fermi energy on a more meaningful scale. In this way, we obtain transport information and, in addition, the energy level alignment at the heterojunction interface. We associate the threshold voltage with the mobility edge of the conduction band. Below the threshold potential V_t, we observe a sharp exponential increase from an intrinsic nonconductive domain up to the formation of the conductive n-channel. It is in this region that we are able to obtain information regarding the in-gap trap states and determine their impact on electronic device properties.[15]

The fabrication of the nanodielectric is depicted in Figure 2a. A patterned aluminum gate is electrochemically oxidized, defining what will become the channel length. We monitor the oxide formation *via* the potentiostatic Faraday current−anodization time scan. The maximum resistance is obtained when the electrochemical process is stopped after saturation (10^4 s), where the oxide growth shields the potential of the working electrode and inhibits further alumina formation.[16] This approach—one that employs a self-limiting strategy to grow the gate dielectric—allows us to build the thinnest possible gate oxide that still permits a sufficiently low gate leakage, and through the choice of oxidation potential, we select the upper limit on the gate voltage that can be applied before breakdown.[17,18] This self-limiting method allows us to grow high-quality gate insulators, among the thinnest used in colloidal quantum dot FETs, without having to use high-temperature deposition methods or postprocessing. To passivate the electron-trapping hydroxyl groups on the bare anodized alumina, we grow an aliphatic self-assembled monolayer (SAM) containing

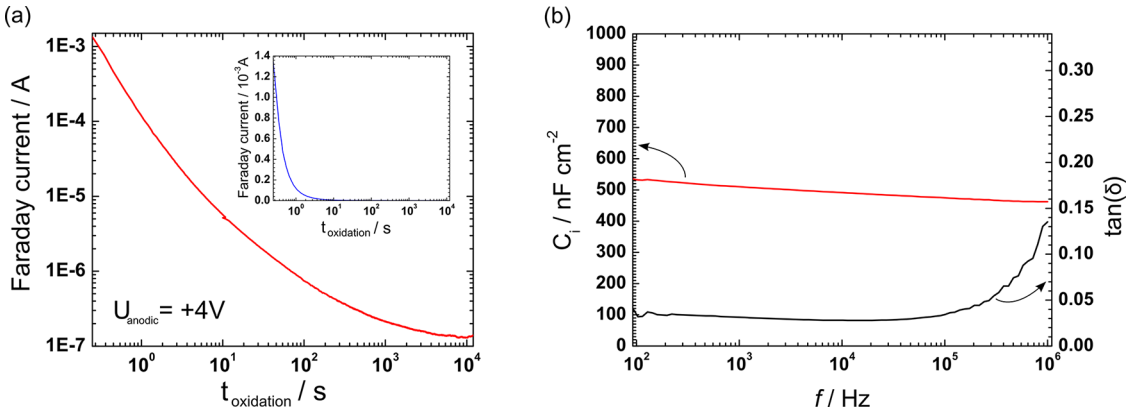

Figure 2. (a) Faraday/oxidation current during oxide growth plotted as a function of anodization time (inset shows the same data plotted on a linear scale). After approximately 10^4 s, the Faraday current is no longer decreasing with time and the electrochemical system is at equilibrium. Our nanodielectric, consisting of 8 nm alumina and a 2−3 nm SAM for an optimized interface, has a geometric capacitance of approximately 500 nF cm^{-2} ± 5.1%. This method enables us to achieve capacitances close to the theoretical value of about 1000 nF cm^{-2} for an 8 nm alumina dielectric. The breakdown voltage of the nanodielectric corresponds to potentiostatic electrochemical growth conditions of +4 V before saturation/equilibrium. (b) Geometric capacitance (C_i) and the breakdown (tan δ) curve plotted as a function of frequency.

the same hydrocarbon chain length (C_{18}) as the oleic acid capping our quantum dots in solution to have ideal interface matching. We grow this monolayer in the gaseous phase to ensure fully sp^3-hybridized hydrocarbon chains for an optimally trap-minimized interface.[19] Without proper surface passivation, as is the case with bare alumina, the FET *IV* characteristics are poor and the subthreshold regime is too broad to analyze (see Supporting Information Figure S3a). OTS was found to be the best passivant resulting in the sharpest onset from the subthreshold to conducting regime, thus the fewest trap states associated with the interface itself (see Figure S3b for a comparison with *n*-octadecylphosphonic acid).

We measured the geometric capacitance of the device, including the additional octadecyltrichlorosilane (OTS) SAM, to be 500 nF cm^{-2} ± 5% (Figure 2b), on par with the best thin dielectrics in CQD FETs.[11,12] This is in good agreement with the ~1 μF cm^{-2} maximum capacitance expected for an 8 nm alumina dielectric layer.

The FET spectroscopy deployed on the nanodielectric typically yields an on/off ratio of 10^4 with the application of only ~2.5 V of gate potential. The nonconductive, subthreshold, and conductive regimes of the FET transfer characteristic are shown in Figure 3a (linear scale) and 3b (log scale).

The conductive regime is defined by the region of linear transport, where the transconductance, $\delta I/\delta V_g$, is constant. Figure 3c shows the FET output curves, demonstrating a clear delineation between the linear and saturation regimes. At a source−drain bias of 100 mV, the FET is operating in the linear regime, in which the mobility, μ_e, is proportional to the transconductance and is given by

$$\mu_e = \frac{1}{C_i V_d} \times \frac{L}{W} \times \frac{\delta I}{\delta V_g} \qquad (1)$$

The threshold voltage, V_t, defines the boundary between the subthreshold and transport regimes, as indicated by the intersection of the slope of the current−voltage transfer characteristic with the *x*-axis (Figure 3a). The subthreshold regime is characterized by the sharp increase in the log(I_{drain}) *versus* V_g plot. It is in this region where the Fermi energy of the quantum dot film at the dielectric interface lies within the band gap. As the gate voltage is increased and the majority carriers are accumulated to form the conductive channel, the Fermi energy is swept through the band gap, toward the conduction band edge, filling in-gap trap states along the way. We obtained a subthreshold swing, *S*, defined as the increase in gate voltage per 10-fold increase in source−drain current, in the range of 250−450 mV decade^{-1}. This value is comparable to the best values reported in CQD FETs[12] and other disordered systems such as organic field-effect transistors.[20,21] We used the subthreshold swing, *S*, and our measured geometric capacitance, C_i, to estimate the two-dimensional trap density within the active region of quantum dots at the interface, $N_{t,2D}$:[15]

$$N_{t,2D} = \left(\frac{S \times e}{k_B T \ln 10} - 1\right) \times \frac{C_i}{e} \qquad (2)$$

In this way, we are able to measure both CQD film mobility and an upper limit to the trap density in the active region as a function of gate bias. It is important to note that mobilities as measured by field-effect transistor studies are decoupled from the effects of in-gap trap states on transport. These trap levels within the band gap are occupied once the Fermi level is at the conduction band edge, which is where the conductive regime occurs and where mobility is subsequently measured.

Accumulation mode FETs probe the majority carriers in doped CQD films. While the minority carriers

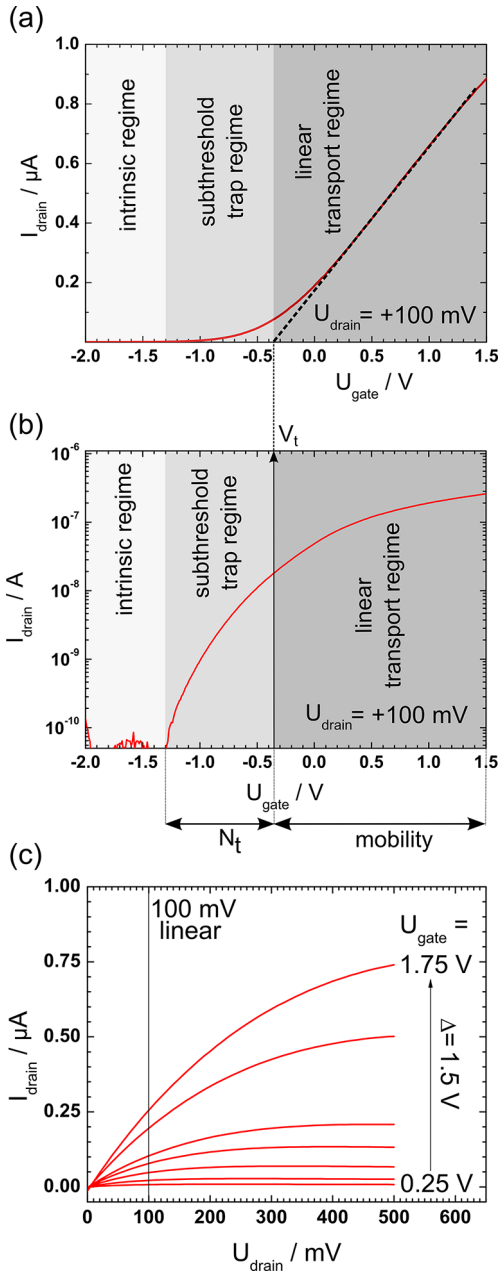

Figure 3. (a) Linear scale transfer characteristic of an iodide dissolved in methanol ligand-exchanged nanocrystal field-effect transistor, highlighting the threshold voltage, V_t, as the intersection of the linear conductance region with the voltage axis. (b) Log scale transfer characteristic, highlighting the intrinsic, subthreshold, and conducting regimes. (c) Output *IV* characteristics showing the linear regime at 100 mV, which is the applied bias for the measurement of mobility.

certainly play a strong role in determining photovoltaic performance metrics, the impact of majority carriers is often neglected. Under typical CQD doping levels in photovoltaic cells of $10^{15}-10^{16}$ cm^{-3},[6,22] the excess carrier concentrations under illumination levels near one sun (~1000 W/m^2) can approach or even exceed the equilibrium carrier density. Under these conditions, the majority carriers have a strong impact in determining the open-circuit voltage.

We apply our trap state density mapping technique to explore the majority carrier energy landscape in several different types of halogen-passivated lead sulfide quantum dot films that have recently demonstrated superior optoelectronic properties in photovoltaic cells.[7] These n-type films form accumulation mode electron channels, and no ambipolar behavior is observed. We explored the effects of changing the ligand and the solvent for the ligand on mobility and trap density. Much work has been done to optimize these parameters empirically using photovoltaic power conversion efficiency (PCE) as the metric of interest. We sought instead to use our FETs as a way to map out both transport and shallow trap density to elucidate the specific roles they play in device performance. We hoped to use this mechanistic insight in order to guide future research directions.

Figure 4 shows the transfer characteristics (a–c, insets are on a linear scale), trap state density (d), and mobility (e) as a function of gate bias for three different solid-state treatments of PbS CQD films.

A mobility-only analysis of these materials (Figure 4e) would have resulted in the conclusion that iodide dissolved in methanol (MeOH) is the best solvent/ligand pair for further optimization in photovoltaic cells and bromide-MeOH-treated films to be the least ideal. However, by analyzing the subthreshold trap-filling regime and mapping out the energy-transport characteristics of these nanocrystal films, we built a more complete picture of film performance. From the subthreshold analysis of trap state density (Figure 4d), it is bromide dissolved in methanol that results in the cleanest band gap and iodide solvated by isopropyl alcohol (IPA) that has the highest trap state density. We found that treatments based on ligands in IPA result in photovoltaic devices that do not perform as favorably as ligands in MeOH. Moreover, films utilizing bromide-MeOH as a ligand consistently resulted in comparable photovoltaic performance to iodide-MeOH, despite having lower mobility. In the case of IPA-solvated ligands, the increased formation of traps limits device applications, despite providing the highest mobility. For methanol-solvated bromide, the reduced trap state density compensates for the decrease in mobility.

CONCLUSIONS

These results can be used to guide future studies in materials engineering for CQD photovoltaics. Specifically, they provide motivation to investigate the wide ligand–solvent parameter space for simultaneously maximizing mobility and minimizing shallow trap state density. Presently, the FET-based shallow trap characterization method can be combined with the photovoltage transient spectroscopy technique[6] to give a broader picture of the density of states within the band gap of a CQD film. Looking forward, this work facilitates

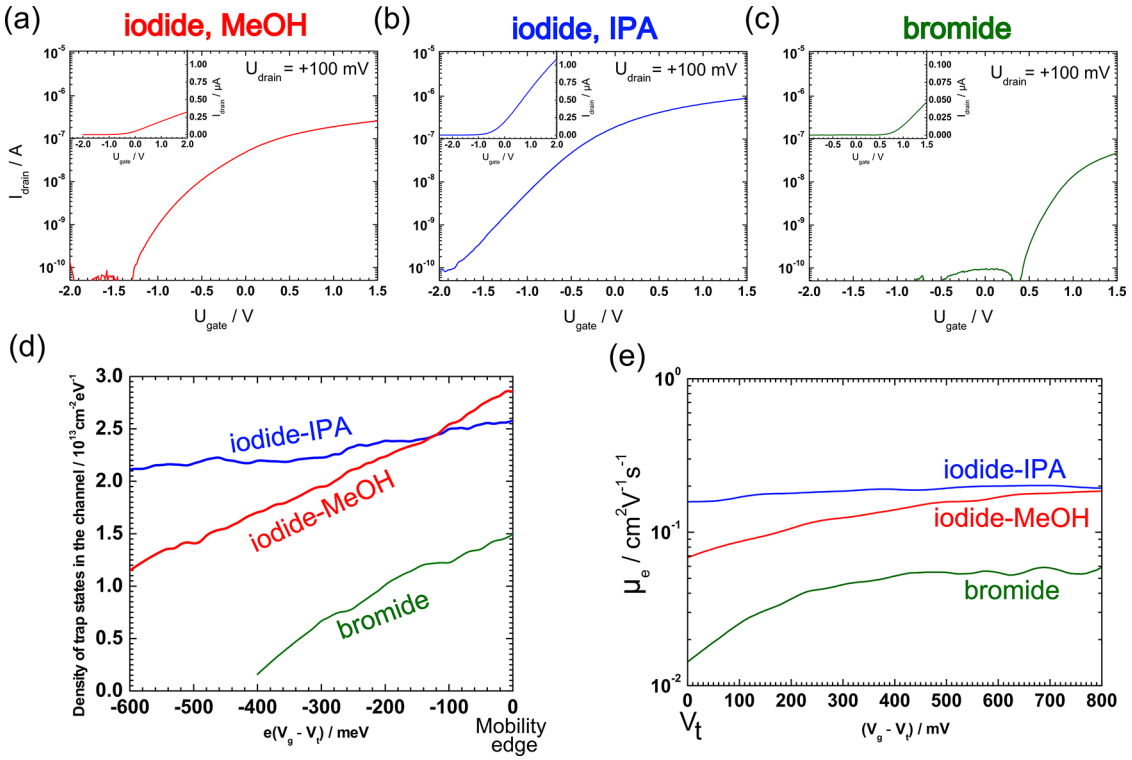

Figure 4. (a) *IV* transfer characteristic of a CQD FET treated with iodide dissolved in methanol. (b) Transfer characteristic for a film treated with iodide solvated by isopropyl alcohol. (c) Transfer characteristic for a film treated with bromide in methanol. (d) Trap state density in the channel as a function of gate bias for the three treatments as calculated by eq 2. We explore the impact of solvent and halide type on the subthreshold trap state density. The change from methanol (MeOH) to isopropyl alcohol (IPA) introduces more trap states, particularly deeper into the gap, while replacement of iodide with bromide led to a more favorable trap distribution in the band gap. (e) Comparison of the mobility characteristics for the three treatments. IPA-treated dots exhibit increased mobility values, whereas treatment with bromide reduced the film mobility significantly.

future studies that further develop the gate voltage to Fermi energy correlation and, additionally, quantify not only the mobility and the trap state density but also the equilibrium free carrier density and its relationship to these parameters.

We have applied this subthreshold analysis to some of our commonly used n-type CQD films to analyze the trap states near the conduction band. The technique could also be applied to a p-type film to analyze the states near the valence band or applied to an ambipolar film to measure the trap states near both energy bands simultaneously. What is required is simply the formation of a conductive channel at the CQD/dielectric interface and that the signal be sufficient to overcome any noise.

We emphasize the importance of considering both trap state distributions and mobility to obtain a more thorough electronic map of CQD films. We demonstrated a low-voltage nanodielectric FET approach that relies on a self-limiting gate oxide growth method to characterize both transport and trap state density within the CQD film. We used our approach to conduct a proof-of-principle study on solid-state treatment methods for CQD films and determine the impact of both mobility and shallow trap state density on photovoltaic performance directly. The resulting picture allows us to identify the most promising routes for future materials engineering paths—an attractive insight for tailoring CQD films for improved optoelectronic device applications.

METHODS

Field-effect transistor (FET) structures were fabricated as follows: The aluminum gate electrode (150 nm) was thermally evaporated onto a glass substrate using an Edwards thermal evaporator. The aluminum oxide layer was grown electrochemically in a 0.01 M solution of citric acid monohydrate in purified deionized water. Four volts was applied between a stainless steel counter electrode and the gate working electrode for 2.5 h using a Keithley 2400 source meter. Afterward, an octadecyltrichlorosilane (OTS) self-assembled monolayer was grown by placing an open vial containing the volatile liquid (5 mL) in a desiccator with the anodized samples for 12 h at 90 °C.

The quantum dots have been synthesized according to a previously reported method.[7] First, 3.3 nm PbS CQDs dissolved in octane (50 mg/mL) were spin-cast onto a glass substrate at 2500 rpm for 10 s under nitrogen in an Innovative Technology glovebox. The samples were soaked for 1 min in a 0.1 M solution of tetrabutylammonium iodide (TBA-I) or TBA-Br in MeOH or IPA.

The source/drain electrodes were deposited using an Angstrom Engineering Amod deposition system in an Innovative

Technology glovebox. For the contacts, titanium (150 nm) was deposited at a rate of 1 nm/s using a stainless steel shadow mask. The FET geometries (W/L) are (2000 μm/33 μm). A Keithley 2400 source meter supplied the gate and source/drain voltages and measured the source−drain and leakage currents. All current−voltage scans were taken at a scan rate of 10 mV per 100 ms of integration time. Scans were done in the direction from negative to positive gate voltage. An HP LCR meter was used to measure the capacitance C_i in a metal oxide/SAM metal sandwich structure, using the same oxidation and passivation procedure as for the FET.

Samples prepared by the above methods were processed for cross-sectional TEM imaging. Using a Zeiss NVision 40 focused ion beam (FIB) mill, thin films (approximately 100 nm) were prepared with a Ga^+ beam then argon-ion nanomilling. For imaging, a FEI Titan 80-300 Cubed STEM equipped with EDS/EELS analyzers was used.

Conflict of Interest: The authors declare no competing financial interest.

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Supporting Information Available: FET shadow mask details, sample *IV* scans showing hysteresis, and the effects of different surface passivation on the FET characteristics. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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